The Hebrew University of Jerusalem

Syllabus

VLSI Hackathon - 83934

Last update 23-09-2024

HU Credits: 2

Degree/Cycle: 1st degree (Bachelor)

Responsible Department: Applied Physics

Academic year: 0

Semester: 2nd Semester

Teaching Languages: Hebrew

Campus: E. Safra

Course/Module Coordinator: Prof. Freddy Gabbay

Coordinator Email: freddy.gabbay@mail.huji.ac.il

Coordinator Office Hours: Coordinate in advance via e-mail

Teaching Staff:

Prof. Freddy Gabbay

Course/Module description:
A hackathon course for developing a hardware accelerator with a RISCV processor

Course/Module aims:
The course will provide the students with a unique experience of an hackathon event which combines a development of hardware accelerator in hardware description language (SystemVerilog / Verilog) with RISCV microprocessor. The course will provide students an in-depth experience on the interaction of microprocessor, an accelerator and the software.

Learning outcomes - On successful completion of this module, students should be able to:
The students will experience developing accelerator hardware together with a RISCV processor in combination with software

Attendance requirements(%):
100

Teaching arrangement and method of instruction: Active learning (project-based learning) through the hackathon that combines several online preparation sessions

Course/Module Content:
1. RISC-V processor architecture
2. Hardware accelerators
3. System-level viewpoint that combines a processor, an accelerator, a hardware card and software

Required Reading:
none

Additional Reading Material:
none

Grading Scheme:

Essay / Project / Final Assignment / Home Exam / Referat 70 %
Submission assignments during the semester: Exercises / Essays / Audits / Reports / Forum / Simulation / others 30 %

Additional information:
The attendance in the hackathon event is mandatory.