



The Hebrew University of Jerusalem

Syllabus

Computer Architecture - 67200

Last update 05-10-2023

HU Credits: 5

Degree/Cycle: 1st degree (Bachelor)

Responsible Department: Computer Sciences

Academic year: 0

Semester: 2nd Semester

Teaching Languages: Hebrew

Campus: E. Safra

*Course/Module Coordinator: Ohad Falik
Ron Gabor*

Coordinator Email: ohadf1@cs.huji.ac.il

Coordinator Office Hours: Sunday 9:00-10:00, Coordinate in advance

Teaching Staff:

Mr. Ohad Falik,
Mr. Ron Gabor,
Mr. Ori Meir,
Mr. yoel olivier

Course/Module description:

The course is an introduction to digital hardware design and computer architecture concepts and design. The following topics will be covered:

1. Introduction to computer Architecture :

[Computer Elements, Moors' law, ISA, Performance, Amdahl law]

2. Number Representation [Integer, fix point and Floating Point – conversion, range and arithmetic]

3. Introduction to semiconductors and transistor as switch. Building logic functions from transistors.

4. Boolean algebra and combinatorial functions. Function minimization. Elementary and advanced logic functions.

5. Combinatorial circuits. State machine taxonomy and concepts. Sequential Circuits and memory elements (latches and flip-flops). Synthesis of state machines.

6. Timing of combinatorial and sequential circuits.

7. HW description language fundamentals

8. Introduction to processor architecture (C to assembly and binary, Van-Neumann vs. Harvard, CISC vs. RISC, architecture compatibility visible-ISA vs. micro-architectural point of views). Execution steps and MIPS Instruction set

9. MIPS Implementation: Single cycle, Multi-cycle, Pipeline (including pipeline principals and hazards). Focus points : performance estimation, trade off understanding, circuit frequency, pipeline hazard elimination), Interrupts

10. Memory hierarchy : problem, terms, taxonomy of misses, cache design, cache behavior under program examples, types of caches (direct, set-associative, fully associative).

11. Virtual Memory : why do we need virtual memory, concepts, page mapping [flat and hierarchical], problems, memory management and TLB issues.

12. Modern Computer Architectures: Parallelization methods, Super pipelining,

Vector Machines, Cache Coherency

13. Selected topics of : prediction methods, IO Operation.

Course/Module aims:

Familiarity with numbers representation methods, hardware elements and hardware design methods.

Understanding the principles of computer architecture and implementation of a simple processor.

Familiarity with advanced topics in architecture.

Learning outcomes - On successful completion of this module, students should be able to:

Design simple hardware systems.

Analyze systems and processors computing systems having different microarchitectures.

Analyze and make optimization to software to match different architectures.

Understand the trade off of different architectural solutions.

Attendance requirements(%):

0

Teaching arrangement and method of instruction: Frontal lectures + frontal exercise lessons + home assignments.

Course/Module Content:

1. Introduction to computer Architecture :

[Computer Elements, Moors' law, ISA, Performance, Amdahl law]

2. Number Representation [Integer, fix point and Floating Point – conversion, range and arithmetic]

3. Introduction to semiconductors and transistor as switch. Building logic functions from transistors.

4. Boolean algebra and combinatorial functions. Function minimization. Elementary and advanced logic functions.

5. Combinatorial circuits. State machine taxonomy and concepts. Sequential Circuits and memory elements (latches and flip-flops). Synthesis of state machines.

6. Timing of combinatorial and sequential circuits.

7. HW description language fundamentals

8. Introduction to processor architecture (C to assembly and binary, Van-Neumann vs. Harvard, CISC vs. RISC, architecture compatibility visible-ISA vs. micro-architectural point of views).

Execution steps and MIPS Instruction set

9. MIPS Implementation: Single cycle, Multi-cycle, Pipeline (including pipeline principals and hazards). Focus points : performance estimation, trade off understanding, circuit frequency, pipeline hazard elimination)

10. Memory hierarchy : problem, terms, taxonomy of misses, cache design, cache behavior under program examples, types of caches (direct, set-associative, fully associative).

11. Virtual Memory : why do we need virtual memory, concepts, page mapping [flat and hierarchical], problems, memory management and TLB issues.

12. Modern Computer Architectures: Parallelization methods, Super pipelining, Vector Machines, Cache Coherency

13. Selected topics of : prediction methods, Interrupts and IO Operation.

Required Reading:

N.A

Additional Reading Material:

"האוניברסיטה הפתוחה" - מערכות ספריות

- Computer Architecture and Design. The Hardware / Software Interface - Hennessy & Patterson

- Computer Architecture a Quantitative Approach - Hennessy & Patterson

- Hennessy, J. L., and D. A. Patterson. Computer Architecture: A Quantitative Approach, 3rd ed. San Mateo, CA: Morgan Kaufman, 2002. ISBN: 1558605967.

Grading Scheme:

Written / Oral / Practical Exam 70 %

Submission assignments during the semester: Exercises / Essays / Audits / Reports / Forum / Simulation / others 20 %

Mid-terms exams 10 %

Additional information:

Home assignments (20%):

Weighted average of home assignments:

- 70%: 10-11 home assignment submitted. Average of top n-2 of the submitted home assignments.

- 30%: two home assignments to be conducted in one interview (no submission).

At least 65 is required in this weighted average.

The mid-term quiz will be taken into account only if its grade is higher than the exam grade. If not than the final exam will be 80% of final grade.

Exam grade of at least 60 is required to pass the course.